

Rev. 03/05/04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Fabrizio Petrini

Docket No.: S-94,651

Serial No.: 09/895,570

Examiner: Wu, Qing Yuan

Filed : 6/28/2001

Art Unit: 2194

For : BUFFERED COSCHEDULING FOR PARALLEL PROGRAMMING  
AND ENHANCED FAULT TOLERANCE

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR 1.56, 1.97, AND 1.98**

Sir:

The documents listed below are identified in compliance with the duty of disclosure defined in 37 CFR 1.56. Copies are attached as appropriate.

1. Diefendorff, "Compaq Chooses SMT for Alpha: Simultaneous Multithreading Exploits Instruction – and Thread-Level Parallelism," Microprocessor Report, Vol. 13, No. 16, December 1999, pp. 1-7.
2. Keckler et al., "Concurrent Event Handling through Multithreading," IEEECS, Vol. 48, No. 9, September 1999, pp. 903-916.

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**CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8(a))**

I hereby certify that this correspondence is, on the date shown below, being:

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Date August 2, 2005

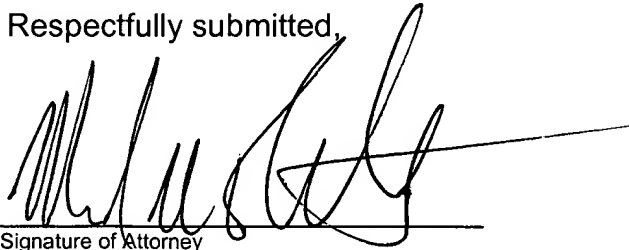
Mark N. Fitzgerald  
(type or print name of person certifying)

3. Tseng et al., "All-to-All Personalized Communication in a Wormhole-Routed Torus," IEEECS, Vol. 7, No. 5, May 1996, pp. 490-505.
4. Arpaci-Dusseau et al., "Scheduling with Implicit Information in Distributed Systems," June 1998, pp. 1-11.
5. Eggers et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors," IEEE Micro, September/October 1997, pp. 12-19.
6. Raz et al., "Dynamic Load Balancing," US Patent 6,173,306, Issued January 9, 2001.
7. Kato et al., "Ring Systolic Array System for Synchronously Performing Matrix/Neuron Computation Using Data Transferred Through Cyclic Shift Register Connected in Cascade of Trays," US Patent 5,600,843, Issued February 4, 1997.

This Information Disclosure Statement is not to be construed as a representation that a search has been made or that additional matter material to the examination of this application does not exist. Applicant does not believe that any of these citations constitutes prior art under 35 U.S.C. 102.

It is requested that the above citations be made of record in the prosecution of this application.

Respectfully submitted,



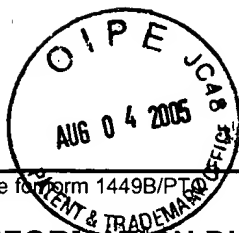
Signature of Attorney

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<sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.



Substitute for form 1449B/PTO		<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>		<i>Complete if Known</i>	
				Application Number	09/895,570
				Filing Date	6/28/2001
				First Named Inventor	Fabrizio Petrini
				Art Unit	2194
				Examiner Name	Qing Yuan Wu
Sheet	2	of	2	Attorney Docket Number	S-94,651

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published (when known)	T <sup>2</sup>
		Diefendorff, "Compaq Chooses SMT for Alpha: Simultaneous Multithreading Exploits Instruction – and Thread-Level Parallelism," Microprocessor Report, Vol. 13, No. 16, December 1999, pp. 1-7.	
		Keckler, et al., "Concurrent Event Handling through Multithreading," IEEECS, Vol. 48, No. 9, September 1999, pp. 903-916.	
		Tseng et al., "All-to-All Personalized Communication in a Wormhole-Routed Torus," IEEECS, Vol. 7; No. 5, May 1996, pp. 490-505.	
		Arpaci-Dusseau, et al., "Scheduling with Implicit Information in Distributed Systems," June 1998, pp. 1-11.	
		Eggers, et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors," IEEE Micro, September/October 1997, pp. 12-19.	
Examiner Signature			Date Considered

<sup>1</sup> Applicant's unique citation designation number (optional).

T<sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.